CLAIMS

What is claimed is:

1. A data optimization engine for optimizing selected frames of a first stream of data, comprising:

a transmit interface circuit coupled to an optimization processor, said transmit interface circuit being configured for receiving said first stream of data, said transmit interface circuit includes

a traffic controller circuit for separating frames in said first stream of data into a first optimizable frame and a first non-optimizable frame, and

an optimization front-end circuit coupled to said traffic controller circuit to receive at least a first portion of said first optimizable frame, said optimization front-end circuit including

a protocol conversion circuit configured to convert data in said first portion of said first optimizable frame from a first protocol to a second protocol suitable for processing by said optimization processor, said first protocol specifies a first word length, said second protocol specifies a second word length different from said first word length, said optimization front-end circuit further includes

an end-of-optimization-file processing circuit, said end-of-optimization-file processing circuit flagging an end of said first portion of said first optimizable frame to said optimization processor,

wherein said optimization processor is configured to optimize said first portion of said first optimizable frame by performing at least one of compression and encryption on said first portion of said first optimizable frame.

2. The data optimization engine of claim 1 wherein said end-of-optimization-file flagging circuit is configured to add, after said data in said first portion of said first optimizable frame is converted from said first protocol to said second protocol, an end-of-optimization-file flag to each word sent from said transmit interface circuit to said optimization processor.

3. The data optimization engine of claim 2 wherein said end-of-optimization flag is one bit long.

4. The data optimization engine of claim 1 wherein said first protocol is the 10-bit interface protocol, and said protocol conversion circuit includes a 10-bit/8-bit lookup table.

5. The data optimization engine of claim 4 further including a frame alignment circuit for detecting and aligning a start of a primitive signal word in said first stream of data with a start of a reference 40-bit word, thereby framing said primitive signal word with respect to said reference 40-bit word.

6. The data optimization engine of claim 5 wherein said frame alignment circuit detects said start of said primitive signal word by monitoring for a K28.5 10-bit word in said first stream of data.

7. The data optimization engine of claim 4 further including an output FIFO coupled to said traffic controller circuit and said optimization front-end circuit, said traffic controller circuit further includes a start-of-frame handler circuit and an end-of-frame handler circuit, said start-of-frame handler circuit is configured detect a start-of-frame 40-bit word in said first optimizable frame and to send said start-of-frame 40-bit word to said output FIFO, effectively bypassing said optimization front-end circuit, said end-of-frame handler circuit is configured to detect an end-of-frame 40-bit word in said first optimizable frame and to temporarily retain said end-of-frame 40-bit word while waiting for said optimization processor to complete optimizing said first portion of said first optimizable frame, said end-of-frame handler circuit is further configured

to furnish a polarity-correct version of said end-of-frame 40-bit word to said output FIFO for appending to first optimized data within said output FIFO, said first optimized data represents a first optimized version of said first portion of said first optimizable frame after being optimized by said optimization processor.

8. The data optimization engine of claim 7 wherein said transmit interface circuit further includes an end-of-optimized-data flag handler circuit coupled to receive second optimized data from said optimization processor, said second optimized data represents a second optimized version of said first portion of said first optimizable frame after being optimized by said optimization processor, said end-of-optimized data flag handler being configured to detect an end-of-optimized data flag in said second optimized data and signals, upon detecting said end-of-optimized data flag in said second optimized data, said end-of-frame handler circuit to furnish said polarity-correct version of said end-of-frame 40-bit word to said output FIFO.